WELL-MATCHED ECHO CLOCK IN MEMORY SYSTEM

Abstract

The present invention is a random access memory device with a well-matched echo clock signal. The dynamic memory storage device includes a controller, a data bus and multiple memory modules. The data bus is coupled to the controller such that data read and data write information is transferred to and from the controller over the data bus. Multiple memory modules are coupled to the data bus and to the controller. Each of the memory module have a driver that produces an echo clock signal on an echo clock pin. The echo clock pin of each memory module is tied to each of the other memory modules and to the controller. In this way, during a read operation of the random access memory device the data bus and echo clock have matched loading conditions.